

WHAT IS CLAIMED IS:

- 1 1. A process for the fabrication of integrated
2 resistive elements with protection from silicidation,
3 comprising:
4 delimiting at least one active area in a
5 semiconductor substrate; and
6 forming at least one resistive region having a
7 pre-set resistivity in said active area;
8 forming a delimitation structure that delimits
9 said resistive region on top of said active area; and
10 providing salicidation protective elements which
11 extend within said delimitation structure and cover said
12 resistive region.
- 1 2. The process according to claim 1, wherein forming
2 said delimitation structure comprises making delimiters
3 having portions set facing one another.
- 1 3. The process according to claim 2, wherein forming
2 said resistive region comprises implantation of a dopant
3 species in said active area between said delimiters.

1 4. The process according to claim 1, wherein making
2 protective elements comprises:

3 depositing a dielectric layer covering said
4 delimitation structure and said resistive region; and
5 anisotropically etching said dielectric layer.

1 5. The process according claim 4, wherein, during
2 anisotropically etching, said dielectric layer is
3 completely removed above said delimitation structure and
4 is partially removed above said resistive region.

1 6. The process according to claim 4, wherein said
2 dielectric layer has a thickness of at least one half of
3 a distance between opposed delimiters defining the
4 delimiting structure.

1 7. The process according to claim 6, wherein said
2 delimiters have a height of approximately one half of said
3 distance.

1 8. The process according to claim 4, wherein said
2 dielectric layer is made of a material selected in the
3 group consisting of: silicon dioxide, silicon nitride, and
4 silicon oxynitride.

1 9. The process according to claim 1, wherein said
2 delimitation structure is made of polysilicon.

 10. The process according to claim 1, wherein forming
said delimitation structure precedes forming said resistive
region.

1 11. A semiconductor wafer comprising:
2 at least one active area;
3 at least one resistor having a resistive region
4 obtained within said active area; and
5 a delimitation structure set on top of said
6 active area to delimit said resistive region.

1 12. The wafer according to claim 11, wherein said
2 delimitation structure is made of a material used in the
3 semiconductor industry.

1 13. The wafer according to claim 12, wherein said
2 delimitation structure is made of a material selected from
3 a group consisting of a dielectric, a semiconductor and a
4 metal.

1 14. The wafer according to claim 12, wherein said
2 delimitation structure is made of polysilicon.

1 15. The wafer according to claim 11, characterized
2 by comprising protective elements which extend within said
3 delimitation structure and coat said resistive region.

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1 16. The wafer according to claim 15, wherein said
2 protective elements are made of a dielectric material.

1 17. An integrated device comprising:
2 a semiconductor body;
3 at least one active area on the semiconductor
4 body;
5 at least one resistor having a resistive region
6 within said active area;
7 a delimitation structure set on top of said
8 active area to delimit said resistive region.

1 18. The integrated device according to claim 17,
2 wherein said delimitation structure is made of a material
3 used in the semiconductor industry.

1 19. The integrated device according to claim 18,
2 wherein said delimitation structure is made of a material
3 selected from a group consisting of a dielectric, a
4 semiconductor and a metal.

1 20. The integrated device according to claim 18,
2 wherein said delimitation structure is made of polysilicon.

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1 21. The integrated device according claim 17,
2 characterized by comprising protective elements which
3 extend within said delimitation structure and coat said
4 resistive region.

1 22. The integrated device according to claim 21,
2 wherein said protective elements are made of a dielectric
3 material.

1 23. A process for integrated circuit fabrication,
2 comprising:
3 defining an active area in a semiconductor
4 substrate;
5 forming a resistive region having a pre-set
6 resistivity in the active area;
7 forming a polysilicon structure which delimits
8 the resistive region;
9 depositing a protective layer over the
10 polysilicon structure and resistive region;
11 etching the protective layer back to expose the
12 polysilicon structure without uncovering the resistive
13 region; and
14 saliciding the exposed polysilicon structure
15 without affecting the pre-set resistivity in the active
16 area.

1 24. The process according to claim 23, wherein
2 forming the polysilicon structure comprises making opposed
3 delimiters having portions set facing one another.

1 25. The process according to claim 24, wherein
2 forming said resistive region comprises implantation of a
3 dopant species in said active area between said delimiters.

1 26. The process according to claim 23, wherein the
2 protective layer is a dielectric layer and the etching is
3 anisotropic.

1 27. The process according claim 23, wherein the
2 etching of the protective layer completely removes the
3 layer above the polysilicon structure and partially removes
4 the layer above the resistive region.

1 28. The process according to claim 23, wherein the
2 protective layer has a thickness of at least one half of
3 a distance between opposed delimiters defining the
4 polysilicon structure.

1 29. The process according to claim 28, wherein the
2 opposed delimiters each have a height of approximately one
3 half of said distance.

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1 30. An integrated circuit fabricated using the method
2 of claim 23.

1 31. A semiconductor wafer fabricated using the method
2 of claim 23.